What is claimed is:

1. A self testing-and-repairing data buffer, wherein while a system is boot up and the control is not yet transferred to an operation system, a test platform is activated for testing data buffers and it is repaired as faults occurs, the data buffer comprising:

a multiplexer; input of the multiplexer being controlled by the test mode signal from the test platform or the test result of the flip flop for selecting normal data or the repairing data from the previous stage (or test bit signal);

a plurality of flip flops for registering data, inputs of each flip flop being connected to an output of the multiplexer; outputs of each flip flop being connected to an buffer rearrange manager;

a repair unit being controlled by the buffer rearrange manager; when a flip flop is damaged, it being used to replace that flip flop;

a buffer rearrange manager having an allocation unit for recording addresses of damaged flip flops in the test mode and the addresses of fault flip flops are rearranged in the repair unit so that the assessing of data is replaced partially or wholly by the repair unit.

2. The self testing-and-repairing data buffer as claimed in claim 1, wherein the flip flops has a working frequency from a gated clock signal.

3. The self testing-and-repairing data buffer as claimed in claim 2, wherein the gated clock signal is formed by integrating a latched write enable signal and a clock signal through a logic gate; wherein the latched write enable signal is generated by latch a write enable signal which controls the data writing of the flip flops and the latch enable signal is generated from the negative edge of system clock signal.

4. The self testing-and-repairing data buffer as claimed in claim 3, wherein the logic gate is an AND gate.

5. The self testing-and-repairing data buffer as claimed in claim 1, wherein the flip flops is a D type flip flops.

6. The self testing-and-repairing data buffer as claimed in claim 1, wherein the multiplexer is a time paired delayed multiplexer, thereby, data

input is synchronous with the gated clock signal.

7. The self testing-and-repairing data buffer as claimed in claim 1, wherein the test mode signal is the test bit signal corresponding to the number of the flip flops, and the least significant bit is feedback to the most significant bit, which is input to each flip flop for determining whether it is in normal condition.

8. The self testing-and-repairing data buffer as claimed in claim 1, wherein the repair unit is installed with flip flops the number of which is less than or equal to the number of flip flops of the data buffer.

9. The self testing-and-repairing data buffer as claimed in claim 1, wherein the buffer rearrange manager further includes a logic gate for integrating the output values of all flip flops as an input selection signal of the multiplexer.

10. The self testing-and-repairing data buffer as claimed in claim 10, wherein the output of the logic gate is used as a selection control signal of a multiplexer of next data buffer, so that as the previous data buffer or net is damaged, the multiplexer is confined only to select the output data from the previous data buffer for forming a network type repairing.

11. A method for operation a self testing-and-repairing data buffer, wherein the self-test is performed each time the system is started and then a test mode signal is generated, comprising the steps of:

entering into a test mode, the test platform generating a test bit signal with all bit being "1" which are input each flip flop;

if all outputs of the flip flops are "0s" it representing at least one flip flop is stuck at "0" and can not change state, then the repairing unit replacing the flip flop;

if all outputs of the flip flops are "1" then the test platform regenerating a "0" bit, the process being performed from the most significant bit to the least significant bit for determining whether all the flip flop can change state; and

if one of the outputs of the flip flops are "1", then the flip flop corresponding to the address of the bit can not change state normally;

a repair unit replacing the damaged flip flop or all flip flops responsive to the record of the allocation unit.